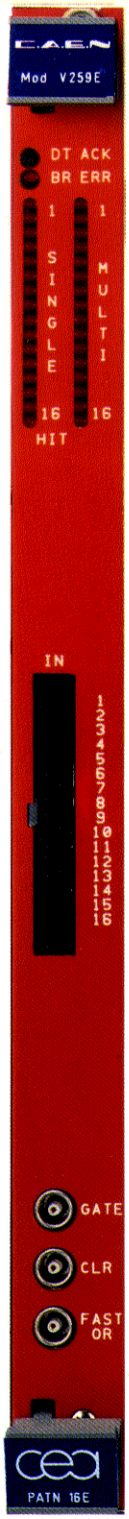
Technical Information Manual

MOD. V 259

16 BIT STROBED
MULTI-HIT PATTERN UNIT

23rd October 1991


C.A.E.N
Mod V259E
DT ACK
BR ERR
1
SINGLE
16
HIT
1
MULTI
16
IN
1
2
3
4
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9
10
11
12
13
14
15
16
GATE
CLR
FAST
OR
PATN 16E

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SECTION 1: INTRODUCTION

The PATN16N module allows the storage of a configuration of 16 NIM signals. An input coincidence circuit commanded by a gate signal selects the data which is placed into a Pattern Register. A Multiplicity Register allows the registering of the presence of multiple bits during the gate signal.

This circuit is realised in a one unit wide standard VME module (figure 1, page 6). It can be read and reset by the VME bus.

1.1 Principal Characteristics

FRONT PANEL

Inputs
16 Standard NIM inputs for the data adapted on 50Ω
One NIM gate input
One fast clear NIM input for the Pattern Register and Multiplicity Register
Minimal width of the input pulses: 4,5 ns

Outputs
Standard NIM level
Fast OR output of the NIM coincidences

Display
Pattern Register on 16 red LED diodes
Multiplicity Regster on 16 red LED diodes
Display of the addressing of the module lasting 1 ms on a green LED diode
Display of the bus errors of the module lasting 1 ms on a red LED diode

PERFORMANCE

Internal 16 channel coincidence, 5 ns minimal width
Minimal resolution in multiple bits: 5 ns

VME INTERFACE

VME A24 D16 protocol
Base address fixed by 4 internal rotary switches
Reading of the Pattern Register and display of its contents by the VME
Reading and reset of the Pattern Register and display of its contents by the VME
Reading of the Multiplicity Register and display of its contents by the VME
Reading and reset of the Multiplicity Register and display of its contents by the VME
Clearing of the Pattern,Multiplicity and Display Registers by a VME command
Clearing of all these registers by SYSRESET
Reading of a module identifier
Reading of the manufacturer identifier

Connectors	All the connectors are coaxial LEMO 00 50Ω	
Power Supply	+ 5V	850 mA
	-12V	370 mA

SECTION 2: GENERAL DESCRIPTION

2.1 Introduction

The PATN16N is a module of data inputs that is designed to register the configuration of 16 NIM level signals. This module can register continuous or impulse levels.

A multiple coincidence circuit selects the input signal during a GATE signal common to the 16 channels. An input signal is considered as "1" logic when this signal is at the level -800 mV during the gate applied to the module. The overlapping between the gate and the input signal must be a minimum of 4 ns.

The output pulse of each coincidence is memorised in a 16 bistables register called "Pattern Register". If the corresponding bistable is already set by a preceding pulse, the corresponding bit of a second register, called "Multiplicity Register", will be set.

One NIM input (CLR) allows the resetting of these registers in the case where you do not wish to keep the information for further reading by the VME bus.

The 16 coincidence outputs are ORed to supply a NIM level signal, available on the front panel (FASTOR). This signal is delayed by 13 ns with respect to the input signals.

A VME interface allows the reading of the Pattern or Multiplicity Registers with or without resetting them. In addition, the reading operation transfers the contents of the corresponding register into a Display Register which allows the observation of the data until the following reading. A particular VME operation other than the SYSRESET bus signal allows the reset of all the registers.

2.2 Front Panel

It conforms to the VME standard of one unit wide. You can find the 16 data inputs, the gate input, the fast clear input and the fast or output other than the display of the last data read. Two other LED diodes indicate the generation of the DTACK and BERR VME signals.

2.2.1 Inputs

The 16 data inputs are situated in the centre and numbered from high to low from 1 to 16. Below you can find the Gate input and clear input (CLR). They consist of 18 coaxial LEMO 00 connectors with a 50 Ω impedance.

2.2.2 Outputs

On the bottom of the panel you can find the or output of the coincidences (FASTOR) on a coaxial LEMO 00 connector 50 Ω.

2.2.3 Display

At the top of the panel you can find one green LED diode which lights up lasting for about 1 ms each time the module emits the DTACK signal on the VME bus. Below, a red LED diode lights up lasting for about 1 ms to indicate a bus error response (BERR) for the time of an addressing cycle of an addressing cycle of the module.

Two columns of 16 red LED diodes display the contents of the Pattern Register (to the left) and of the Multiplicity Register (to the right) read by the last operation on the VME bus. Note that these diodes are active at the moment in which the Pattern and Multiplicity Registers are read.

2.3 Internal Organisation

This module is principally realised in TTL "FAST" logic. It is represented in diagram form in figure 2. The corresponding connections for the functioning attached to the fast electronics are represented by a simple line; those corresponding to the VME access are represented with a double line.

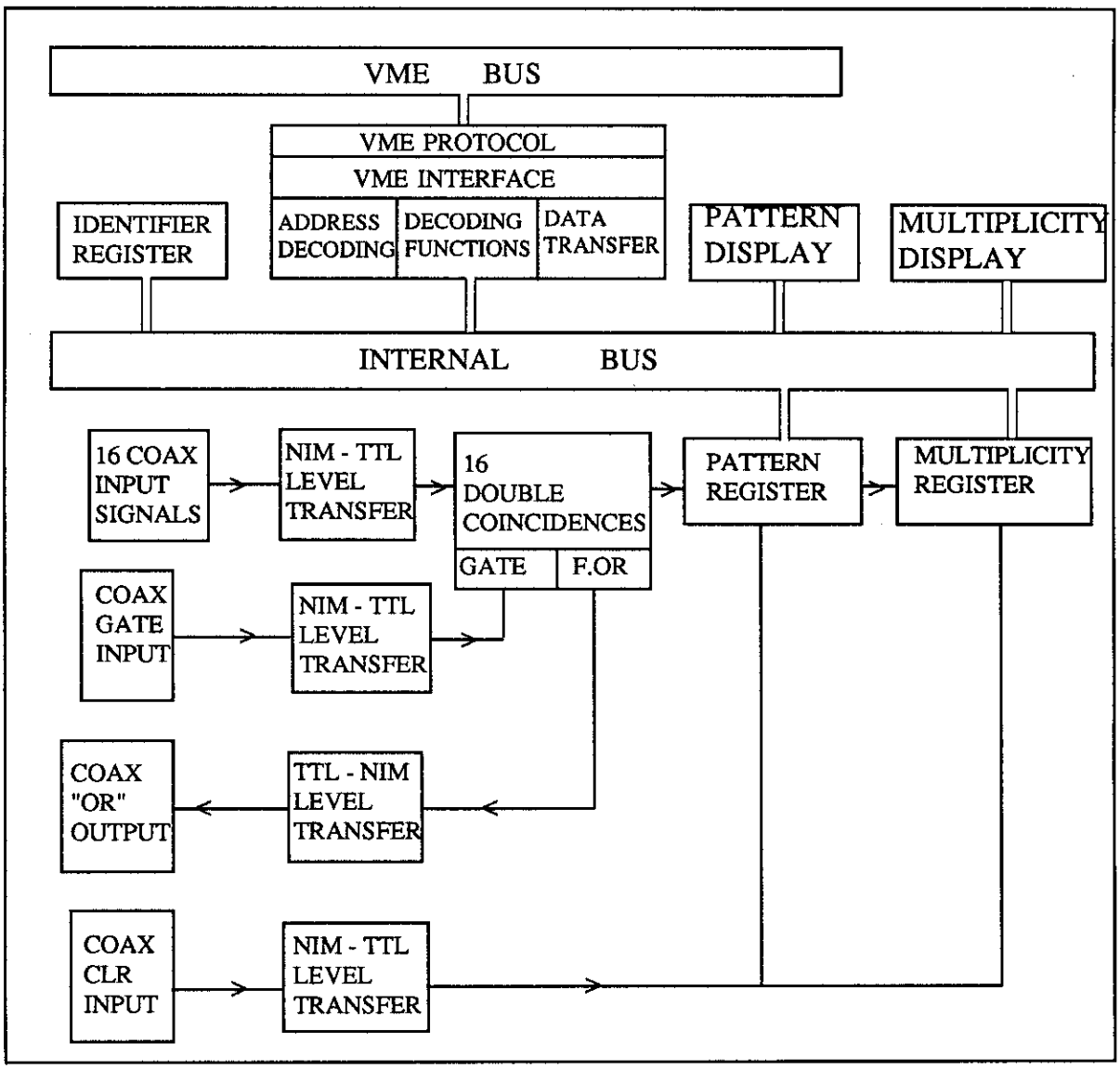

Figure 2. The principal elements of the PAT16N

2.3.1 Inputs and translation of NIM/TTL level

Each NIM data signal enters on the LEMO 00 coaxial connector with an internal adaptation by a 50Ω resistor. The NIM/TTL level translation is made in two stages. The NIM signal is translated in order to be ECL compatible. Then an ECL/TTL translator supplies a TTL output which is applied to the coincidence circuit.

The 16 inputs give the information to be memorised, one gate input enables the selection of the information to be memorised and one fast reset enables the clearing of the memorised information.

2.3.2 Coincidence

It is composed of 16 double coincidence circuits which perform a coincidence of each input signal and the common gate signal. The minimum width of the coincidence curve to half-height is 5 ns. The maximum dispersion between the channels is less than 0,5 ns. The output signal is sensibly equal to the recover between the input signal and the gate signal.

2.3.3 FASTOR Output and translation of TTL/NIM Levels

The output pulses of the coincidences are ORed to supply a NIM signal available on the FASTOR output. The transfer of TTL/NIM level is made usually in two stages: a translation TTL/ECL then a translation ECL/NIM. The nominal 16 mA output signal on a LEMO connector gives a NIM level on a load of 50Ω.

2.3.4 Pattern Register and Multiplicity Register

The output signal of each coincidence is memorised in a latch. The 16 latches form the Pattern Register. The output of each latch commands a JK flip-flop whose clock pulse is supplied by the coincidence signal.

On each channel the first coincidence pulse sets the corresponding bistable of the PatternRegister. If another coicidence occurs, during the gate, the JK flip-flop will clock the "1" of the bistable, thereby indicating that more than one pulse has occurred on that channel during the gate. One reset, coming either by the the CLR input or by VME (reading with reset or specific command) is necessary in order to restart up the process. Note that if several gate signals are sent subsequently without resetting, the circuit will memorise the group of inputs to "1" of the different events.

2.3.5 Reading

On using the internal bus, the reading of the Pattern Register or the Multiplicity Register will apply the corresponding data on the VME bus and will transfer their contents into the visualising register.These data will remain fixed on the two columns of 16 red LED diodes until the following reading. The reading can be made with or without resetting the corresponding registers (see VME Interface).

2.3.6 VME Interface

The module works in A24 D16 mode; this means that the module address must be specified in a field of 24 bits and that the data will be available in words of 16 bits.

The Address Modifiers used authorise the modes of standard addressing in the Data Space in Supervisor Mode or in User Mode.

The module's base address is fixed by 4 rotary switches situated on a subsystem on the printed circuit (figure 6, page 28).

This base address reserves in this way a page of 256 bytes for each module. The use of the addresses in the page is represented in figure 3, page7.

A writing cycle of one word (RAZVM) at the address BASE+$20 resets the two Acquisition Registers, and the two Display Registers. The data are not used.

A reading cycle of one word at the address BASE+$22 reads the Pattern Register, at the address BASE+$24 reads the Multiplicity Register, with resetting of the corresponding register after the reading.

. A reading cycle at the address BASE+$26 reads the Pattern Register, at the address BASE+$28 reads the Multiplicity Register (without resetting).

The two words to the higher address on the page are used to identify the module:

BASE+$FC

15 — 10	9 — 0
Manufacturer N°	Type of module
(*)	(**)

BASE+$FE

15 — 12	11 — 0
Version	Module's serial number

In addition to the address BASE+$FA you can find two particular bytes allowing the confirmation of the presence of the identifier:

BASE +$FA

15 — 8	7 — 0
$FA	$F5

The BERR signal (bus error) will be generated if a reading cycle is effected to the address $20 or if a writing cycle is effected to the addresses $22, $24, $26, $28, $FA, $FE, $FC. This BERR signal will be set furthermore for all the addressing in byte or in double word and for all addressing to the addresses not used on the page.

(*) 000010b
(**) 0000000100b

ADDRESS	DATA/FUNCTIONS
HFE	Version (D15/D12) Series (D11/D0)
HFC	Manufacturer (D15/D10) [*]Module's type (D9/D0) [**]
HFA	HFAF5 (fixed code)
HF8 . . . H2A	**UNUSED**
H28	READs Multiplicity Register
H26	READs Pattern Register
H24	READs &RESET Multiplicity Register
H22	READs &RESET Pattern Register
H20	RESETs all the registers
H1E . . . H00	**UNUSED**

NOTE:
Any attempt to access an unused address will give a BERR (BUS ERROR) signal.

[*] Manufacturer = 000010

[**] Module's type: -NIM = 0000000011
-ECL = 0000000100

Figure 3. Use of the addresses

2.4 Programming

In case of functioning with a CPU board using a 68000 type microprocessor, the access to the module will be made in general with a MOVE.W instruction.

To perform the reset, the destination will be equal to the base address of the module increased by $20. You will avoid the CLEAR instruction which, on certain 680xx, is composed of a reading cycle followed by a writing cycle; the reading cycle should cause the emission of a BERR.

To read a register, the source address will be equal to the base address increased by $22, $24, $26 or $28 for the Multiplicity and Pattern Registers, or $FA, $FC, $FE, for the identifiers.

For other types of microprocessors, memory access instructions will be used: in writing for the reset to zero, in reading in order to access the different registers.

SECTION 3: UTILISATION

3.1 Generalities

Two aspects are to be considered: the fast electronic functions, accessible on the front panel, which carry out in real time independently from VME bus and the functions on the bus. The user must take all the necessary precautions to avoid the interferences in these two module accesses. One has to avoid, in particular, the storage of a configuration by the presence of a gate signal, while the bus effects the reading of one of the registers.

An external logic must assure the correct interlacement between the execution of the operations relative to the front side and those relative to the bus VME (see 3.3.5).

3.2 Put in service

Before inserting the module in the crate you must fix its base address with the aid of the rotatory switches verifying that it is situated in a free zone of the memory space of the microprocessor. It must be different for each module present in the same system. Note that the 256 bytes following the base address are reserved for this module.

Avoid introducing the module until the crate is under voltage.

3.3 Put into operation the front panel

All the front panel signals, NIM standard, are connected by the coaxial LEMO 50Ω connectors; the inputs are internally adapted, the output FASTOR supplies a current of 16 mA. It is not internally adapted

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3.3.1 Input Signals

Apply a NIM signal with a minimum width of 5 ns on each of the inputs to be used. The inputs not used will be registered as zero.

If possible, always apply a short signal on the data inputs.

3.3.2 Command Signals

Apply a gate signal to the corresponding input. The width will be at least equal to the time dispersion of the signals to be memorised. If the states must be memorised, the state memorised is sampled on the front side of the gate signal; if the state passes from "0" to "1" during the duration of the gate, it will be memorised as a "1"; whereas if it passes from "1" to "0", the state "1" will remain memorised.

In using the FASTOR output, you must trace the coincidence curves between the gate and the data signals. Choose for each input the delay required in order that the signal is well centred in the gate; increase eventually the gate width.

If you want to use the CLR, this signal must be issued in time to the exterior of the gate; on the contrary, the module should memorise the states of the signals present between the end of the CLR signal and the end of the gate.

3.3.3 Bus Role

The VME allows the access of the module in two different ways.

In starting up an acquisition program, the reading of the identification registers allows the control of the presence of the modules to the foreseen address. You can usually build a data base where the historic use of each module is held daily. This reading can also be useful for setting right the programmes.

In the acquisition program itself, the VME bus allows the reading of the contents of the acquisition registers, to transfer their contents into the visualising register and reset the acquisition registers.

3.3.4 Data Format

The signals present on the I1 to I16 inputs will be read respectively in 16 bit words, to the addresses ADB+$22 or ADB+$26, on the bits with positions 0 to 15 (I1 on 0, I2 on 1, etc.). The bits 0 to 15 read on the addresses ADB+24 or ADB+28 correspond to the bits on the I1 to I16 inputs.

3.3.5 Timing

On leaving, the PATN has its acquisition registers to zero; its visualising registers contain the data of the last acquired events.

In general, the logic of the operations to be effected for each acquisition is the following:

- open the gate by a low state on the gate signal,
- during its duration, the signals present on the I1 to I16 will be registered,
- the gate signal remounts, that which stops the gate
- in the case, to apply the signal of reset to zero (CLR) of a minimal duration of 5 ns,
- if not, if you want to acquire the memorised data, inhibite the gate signal and carry out the desired VME operations: reading with reset to zero or reset to zero only in the case where the data are not interesting,
- Free the gate signal in order to be able to carry out a new acquisition cycle

3.4 Logic

The base address of the module having been chosen as indicated in paragraph 3.2, you will define

the correspondence between the absolute value of these addresses and their symbolic names used in the programmes.

3.4.1 Registers

Figure 4 describes the registers accessible by logic the answers and the performed functions.

Address	Mode	Answer	Performed function
Base+$20	Write Read	DTACK BERR	CLR,VM, resets all the registers No action
Base+$22	Read Write	DTACK BERR	Reading Pattern Register with reset No action
Base+$24	Read Write	DTACK BERR	Reading Multiplicity Register with reset No action
Base+$26	Read Write	DTACK BERR	Reading Pattern Register No action
Base+$28	Read Write	DTACK BERR	Reading Multiplicity Register No action
Base+$FA	Read Write	DTACK BERR	Fixed code $FAF5 No action
Base+$FC	Read Write	DTACK BERR	version (D15/D12), serial n° (D11/D0) No action
Base+$FE	Read Write	DTACK BERR	Manufacturer (D15/D8), type n° (D7/D0) No action

Figure 4. Register addresses and performed functions.

3.4.2 Initialisation

At power-on the Acquisition and Display Registers can take any state. The emission of the SYSRESET command on the bus resets the group of modules. If this command is not possible due to other modules present in the crate, the command RAZVM can be used to set each module individually. It is also possible to reset the Acquisition Registers by a signal on the CLR input, the updating of the visualisation registers is made from the first reading.

SECTION 4: DETAILED DESCRIPTION

4.1 Introduction

The module is composed of two interlaced systems: a first system of circuits functions under the action of the signals entering on the front panel, it works in real time and it captures the information concerning the trigger electronic. The second group works under the control of the VME bus and assures the reading of the data registered by the acquisition system; it works in delayed time and an external logic must assure the correct interlacement of the two actions.

4.2. Real Time System

It comprises the data inputs (I1 to I16), the command inputs (GATE, CLR), the level transfers, the Pattern Register and the Multiplicity Register.

4.2.1. Inputs and level transfers

The 16 inputs (I1 to I16) are affected by the memorised information, a gate input allows the selection of the memorised information and a fast reset (CLR) allows the clearing of the memorised information.

The data or command signals, at NIM level, enter on the coaxial connectors LEMO 00 and are adapted by internal 50Ω resistors. The translation of NIM/TTL level is made in two stages. The signal NIM is applied on the base of a transistor NPN 2N918 (T1 to T16,T17, T18). The output is taken from the emitter, which allows theshifting of the level of -700 mV. The excursion NIM 0/-800 mV is decreased to -700mv/-1500 mV, compatible with the standard ECL levels. These signals enter on the ECL/TTL translators 10H125 (ICI to IC4) whose TTL outputs are applied to the coincidence circuits.

4.2.2 Coincidence

The coincidence of each input with the common gate signal is made by 4 74F00 (IC11, IC14, IC17, IC20). The minimal width of the coincidence curve at half-height is 5 ns. The maximum dispersion between the channels is about 0,5 ns.

4.2.3 "FASTOR" output

The output pulses of the concidence are mixed to supply a NIM signal available on the "FASTOR" output. The mix is made in two 74F30 (IC28, IC33) and a 74F32 (IC35). The translation of TTL/NIM level is made usually in two stages: a TTL/ECL translation in a 10H124 (IC36) then an ECL/NIM translation in a differential pair of two 2N918 (T19 and T20) of which the two bases are connected by the complementary signals coming from the 10H124 outputs. The output signal, available on the transistor collector, is 16 mA nominal and exits on a LEMO connector. It gives a NIM level on a load of 50Ω.

4.2.4 Storage in the registers

Each signal exiting from a coincidence is connected to the input "set" of a bistable 74F74. On each channel, the first pulse issued from a coincidence sets the D flip-flop and it will therefore be memorised. The 16 bistables 74F74 (IC10, IC12, IC13, IC15, IC16, IC18, IC19, IC21) form the Pattern Register. The "Q" output of each 74F74 commands a JK flip-flop, 74F112 (IC25, IC26, IC29, IC30, IC31, IC32, IC34), where the clock pulse is supplied by the coincidence signal. If another coincidence is produced during the gate, the JK flip-flop is set and remains, indicating that more than one pulse has arrived on this channel during the gate. A reset, either from CLR input or VME is necessary to restart the process.

4.3 Functions connected to the VME bus

4.3.1 Addresses decoding

The MSB of the address (A23 to A4) are decoded in a sub-system (see appendix A) which gives 16 enables (GR0 to GR15) and an output which signals that the base address is valid.

The 16 bits A23 to A8 are used to define the base address of the module and reserve in this way a page of 256 bytes to each module. The 4 bits following are decoded in a demultiplexer which supplies 16 signals defining the groups of 16 bytes. The use of the addresses in the page of the module is represented in figure 3, page 11. The LSB (A3, A2, A1) are applied through the receiver 74F244 (IC53) to the PAL 22V10 (IC52) which decodes the used functions. The Address Modifiers, AM5 to AM0, are decoded in the PAL 20L8 (IC48 see appendix A) which supplies a signal INAM sent to the decoding PAL. This PAL 20L8 also supplies to the decoding PAL the signal MELBER when an unused address group is accessed with a valid Address Modifier.

4.3.2 Decoding functions

The available functions are decoded in the PAL 22V10 (IC52). For the elaboration of these signals, the circuit uses:

the signals IACK, WRITE, LWORD of VME bus
the signals INDSO, INDS1, INA1, INA2, INA3 which are the VME bus signals after passing through the receiver 74F244 (IC53)
the GR2 and GR15 signals coming from the sub-system of address decoding
the signal INAM coming from the PAL IC48.

The VMERAZ signal is generated at the moment of a word writing cycle when IC52 detects ADVAL2 with INA1, INA2, INA3 to zero.

The LECPU signal is generated at the time of a word writing cycle when IC52 detects ADVAL2 with INA1, INA2, INA3 to the value 2 or 6.

The LECMH signal is generated at the time of a word reading cycle when IC52 detects ADVAL2 with INA1, INA2, INA3 to the value 4 or 8.

The VMERZPU signal is generated at the time of a word reading cycle when IC52 detects ADVAL2 with INA1, INA2, INA3 to the value 2.

The signal VMERZMH is generated at the time of a word reading cycle when IC52 detects ADVAL2 with INA1, INA2, INA3 to the value 4.

The LECIDEN signal is generated at the time of a word reading cycle when IC52 detects ADVAL15 with INA1, INA2, INA3 to the value $A, $C, $E.

4.3.3 Data transfer

The different registers communicate with the internal bus through three state circuits.

Reading data and display

The LECPU, LECMH signals generated by IC52, enable the 74F244, IC42, IC44, or IC39, IC43 which assure respectively the connection of the Pattern and Multiplicity Registers on the internal bus. These signals are used as clocks to write the data read into the Display Registers (74F273), IC38, IC45, IC24, IC41. The LED diodes are driven by the 74LSO5A (IC5, IC6, IC7, IC8, IC9, IC42).

Reset of the registers

The reset can be made only when the data have been received by the reading processor. The reset signals (VMERZPU, VMERZMH) are delayed with respect to the reading signals (LECPU, LECMH) by the signal DSR which is obtained in delaying of 25 ns in a 74LS31 (IC56) the mix of the signals INDSO and INDS1 realised in the 74F00 (IC54). The VMERZPU and VMERZMH signals are inhibited during the reading by LECPU and LECMH in the gates IC54/3 and IC54/4 (74F00). This allows the formation of the RAZPU and RAZMH signals after reading of the Pattern and Multiplicity Registers.

A VMERAZ signal is generated at the time of writing to the address BASE+$20. This signal, mixed to SYSRESET in a 74F08 (IC22/4) allows the resetting of all the PATN16N registers.

Identifier reading

The LECIDEN signal (GR15) assures the connection on the internal bus of the PAL 16L8, IC51, IC55 which contains the identification words. The internal address signals INA1, INA2 and INA3 allow to access each of the three addresses $FA, $FC, $FE.

4.3.4 Protocol generation

A VALEC signal, generated by the PAL IC52, assures the connection, in reading, of the internal bus on the VME bus.

In answer to a valid operation, the INDTACK signal is generated through an open collector circuit IC37/2 (74F38) which drives DTACK on the VME bus. This signal is delayed in order that the data be stabilised on the bus.

At the time of an invalid operation, (unused address, long word or byte...) the INBERR signal is generated through an open collector circuit IC37/4 (74F38) which drives BERR on the bus.

These two signals trigger the monostables NE555 (IC46, IC47) which allow the display of these signals lasting for about 1 ms on the LED diodes (green for DTACK and red for BERR). This duration is fixed by the R64, Ch2 for DTACK and R63, Ch1 for BERR.

4.4 Display of register contents

4.4.1 Pattern Register

Two bars of 8 red LED diodes are soldered on the edge of the module's board; two networks (RS1 and RS2) of 330Ω determine the current in the diodes.

4.4.2 Multiplicity Register

The display is on a sub-system board attached to the principal board by the aid of a bar of 17 contacts.

Two bars of 8 red LED diodes are soldered onto the edge of the subsystem board; two networks (RS3 and RS4) of 330Ω determine the current in the diodes.

4.5 Power Supply

The PATN16N uses the voltages +5V and -12V supplied by the VME bus. The -5V used for the power supply of the ECL circuits is produced by an integrated regulator MC7905 (RG1).

SECTION 5: TEST AND ADJUSTMENT PROCEDURES

5.1 Test principles

The test consists of presenting known data in the inputs and verifying that the performed reading in the bus corresponds to the configuration present in the inputs, for different delays between the data and the command signals.

The correct functioning of each channel and the absence of "cross-talk" between the channels on theslow signals (>20 ns) will be studied first. In the second phase, the same information will be measured on fast pulses (5 ns) whose relative phases will vary. In this way the coincidence and resolution curves will be traced.

5.2 Material to put into action

The test block diagram is represented in Figure 5. This system must be controlled by the processor used in the VME crate. This processor handles the sequence of the signals on the front panel and reads the results on the VME bus.

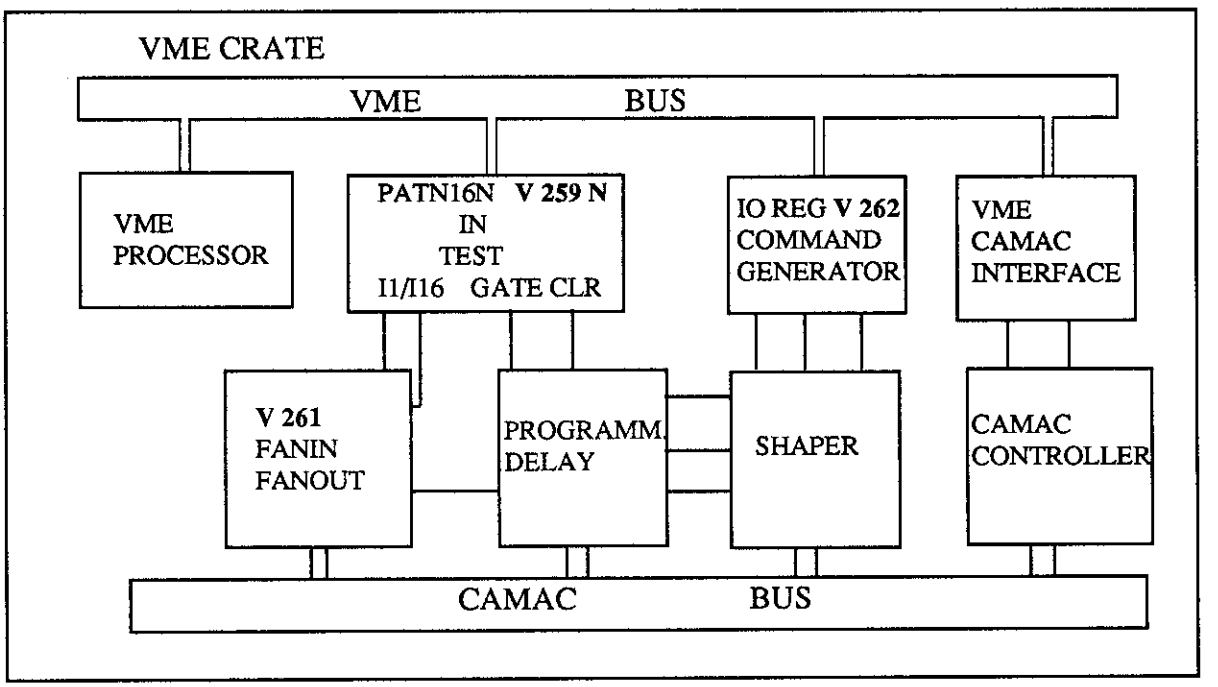


Figure 5: Test Block Diagram

A VME module, IOREG (V 262), allows the CPU to generate three signals towards a shaper which sets their width. The outputs of the shaper cross programmable delay lines. The CLR and GATE signals go directly to the corresponding PATN16N inputs. The third signal is sent on a programmable fanin-fanout (V 261) whose outputs are connected to the PATN16N inputs. For reaons of availability, certain modules are in CAMAC; a VME/CAMAC interface allows the coupling between the two systems.

APPENDIX A:
CHARACTERISTICS OF THE ADDRESS DECODING SUBSYSTEM.

The MSB of the address (A23 to A4) are decoded in this subsystem. The 16 bits A23 to A8 are used to define the base address of the module and reserve in this way a page of 256 bytes for each module. The following 4 bits are decoded in a demultiplexer which generates 16 signals defining internal groups of 16 bytes (GR 0 .. GR 15).The organization of the address decoding subsystem is shown in the following figure.

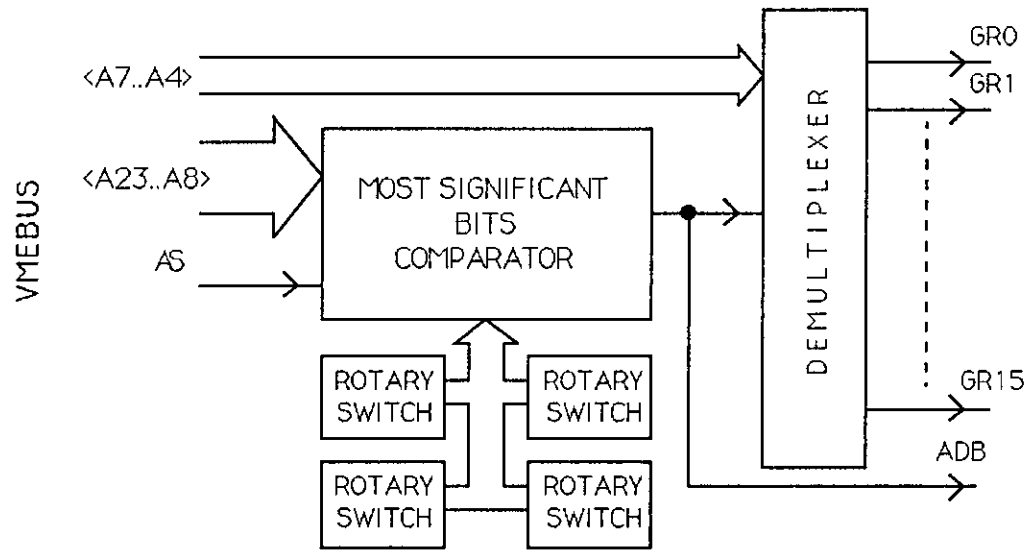


Fig. A.1: Organisation of the address decoding subsystem

The three remaining address bits (A3 to A1), and all the exchange signals with the VMEbus, will be treated in the circuits which are specific for each module.

A.1 Base decoding of the module's address

The decoding of the module's base address is performed by using two comparators 74F521 that comparate the value sets on the four hexadecimal rotary switches with the value of the VME address lines A23 to A8. The comparison is enabled by the AS signal to generate the base address signal (ADB).This signal indicates that the module is accessed by VME.
Each rotary switch sets the value of 4 bits of the module's Base address. Figure A.2 on the following page shows the correspondence between the switches and the address bits.

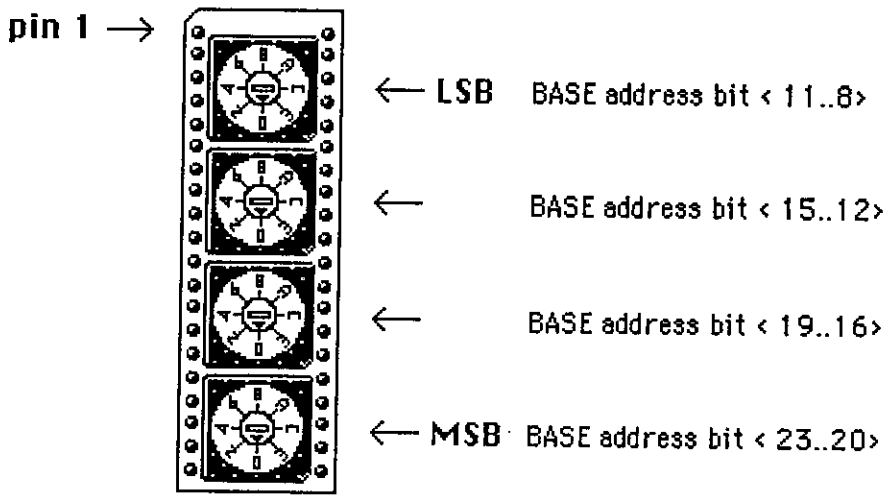


Fig. A.2 : front view of the address decoding subsystem

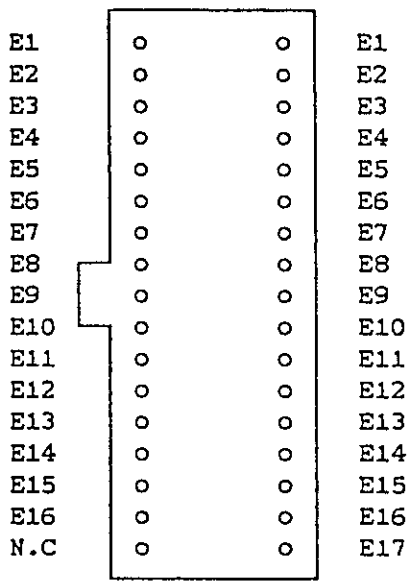
A.2 Decoding of the internal groups

The address lines A7 to A4 are demultiplexed in 16 groups of 16 bytes each, by 2 74LS138 circuits enabled by the base address (ADB).They generate the 16 signals GR0..GR15.

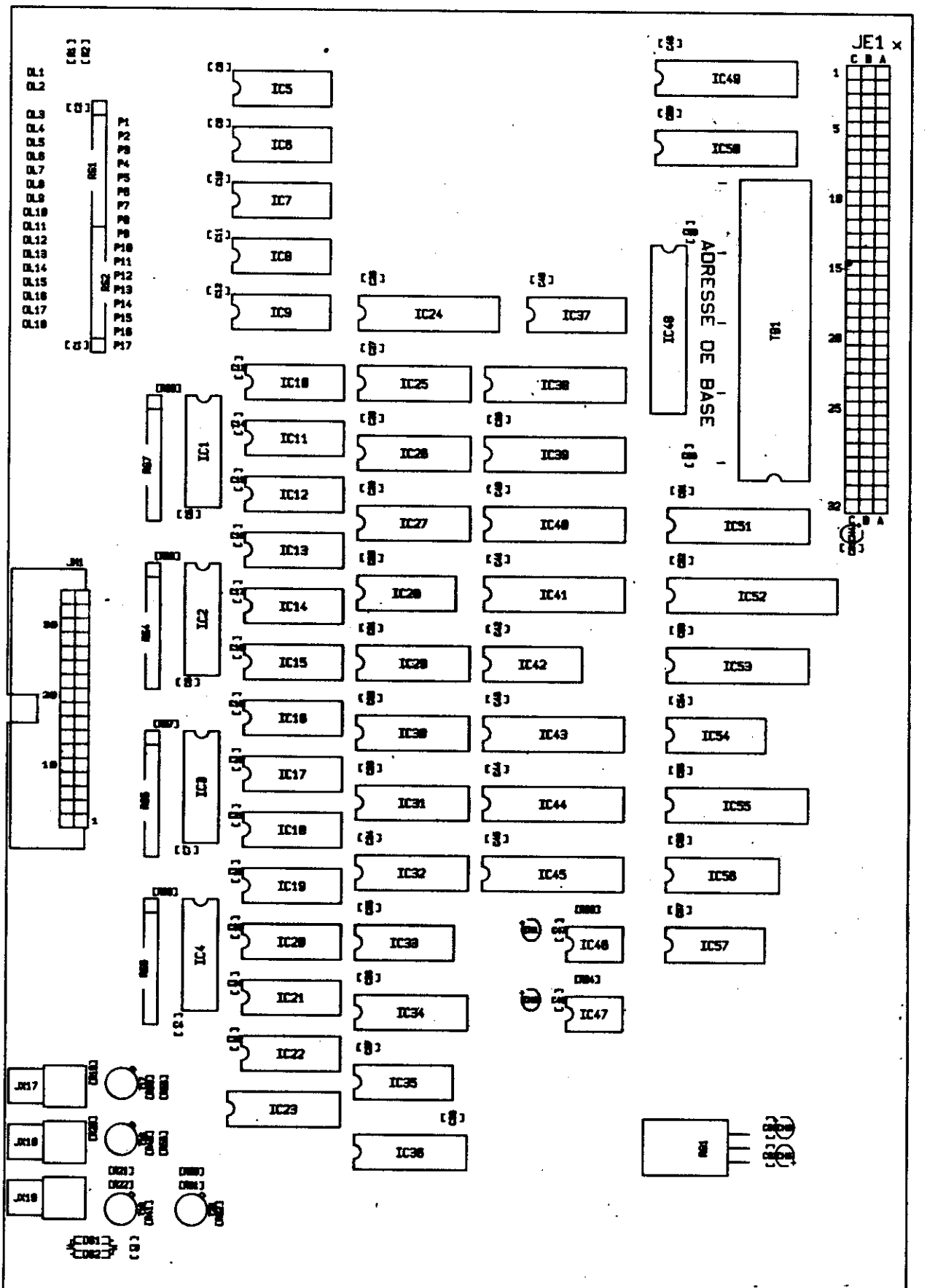
CONNECTOR CABLING

Input connector on the front panel

34 connector contacts seen on the front panel, the contacts are used as follows:



Inputs at "0" -1,7 V -0.9 V
Inputs at "1" -0,9 V -1,7 V


JE1
ADRESSE DE BASE
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC16
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IC48
IC49
IC50
IC51
IC52
IC53
IC54
IC55
IC56
IC57
TB1
RS1
RS2
RS3
RS4
RS5
RS6
RS7
RS8
JM1
JM17
JM18
JM19